AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element circuit fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

an electrically conductive unbiased layer provided on a back side of said substrate ~~for removing~~, said layer being adapted to receive an electric charge related to unwanted voltages and electrical noise from a first region of said substrate and return an electric charge to a second different region of said substrate to maintain a uniform bias voltage throughout the substrate.

2. (Original) The semiconductor device of claim 1, wherein said electrical element comprises at least one electrical element selected from the group consisting of transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

3. (Canceled)

4. (Original) The semiconductor device of claim 1 further comprising a plurality of conductive plugs for respectively coupling said bias voltage source to said distribution regions.

5. (Original) The semiconductor device of claim 1, wherein said conductive layer comprises a conductive metallic layer.

6. (Original) The semiconductor device of claim 5, wherein said conductive metallic layer has a thickness of less than or equal to 10 mil.

7. (Original) The semiconductor device of claim 5, wherein said conductive metallic layer is secured to the backside of said substrate with a conductive adhesive.

8. (Canceled)

9. (Original) The semiconductor device of claim 5, wherein said conductive metallic layer has a resisitivity less than 1×10^{-8} Ohm-meter.

10. (Original) The semiconductor device of claim 5, wherein said conductive metallic layer comprises at least one material selected from the group consisting of copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

11. (Original) The semiconductor device of claim 10, wherein said conductive metallic layer is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

12. (Original) The semiconductor device of claim 5, wherein said metallic layer has at least one length which exceeds a length of said substrate.

13. (Original) The semiconductor device of claim 1, wherein said conductive layer comprises a cured conductive paste.

14. (Original) The semiconductor device of claim 13, wherein said conductive paste has a thickness of less than or equal to 1 mil.

15. (Original) The semiconductor device of claim 13, wherein said conductive paste has a resistivity less than 1×10^{-5} Ohm-meter.

16. (Original) The semiconductor device of claim 13, wherein said conductive paste comprises a material with conductive particles therein.

17. (Original) The semiconductor device of claim 16, wherein said conductive particles comprise at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

18. (Original) The semiconductor device of claim 1, wherein said conductive layer comprises an isotropically conductive polymeric film.

19. (Original) The semiconductor device of claim 18, wherein said conductive polymeric film has a thickness greater than 1 mil.

20. (Original) The semiconductor device of claim 18, wherein said conductive polymeric film has a resistivity less than 1×10^{-5} Ohm-meter.

21. (Original) The semiconductor device of claim 18, wherein said conductive polymeric film comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

22. (Original) The semiconductor device of claim 1, wherein said conductive layer comprises a conductive metallic film.

23. (Original) The semiconductor device of claim 22, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

24. (Original) The semiconductor device of claim 22, wherein said conductive metallic film has a resistivity less than 1×10^{-5} Ohm-meter.

25. (Original) The semiconductor device of claim 22, wherein said conductive metallic film comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

26. (Original) The semiconductor device of claim 25, wherein said conductive metallic film is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

27. (Original) The semiconductor device of claim 1, wherein said device is a memory device.

28. (Original) The semiconductor device of claim 27, wherein said memory device is a dynamic random access memory (DRAM) device.

29. (Original) The semiconductor device of claim 1, wherein said device is a logic device.

30. (Original) The semiconductor device of claim 1, wherein said device is a processor device.

Claims 31-65 (Canceled)

66. (Currently Amended) A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

an electrically conductive unbiased layer provided on a back side of said substrate ~~for removing~~, said layer being adapted to receive an electric charge related to unwanted voltages and electrical noise from a first region of said substrate and return an electric charge to a second different region of said substrate to maintain a uniform bias voltage throughout the substrate.

67. (Original) The system of claim 66, wherein said electrical element comprises at least one electrical element selected from the group consisting of: transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

68. (Canceled)

69. (Original) The system of claim 66, further comprising plurality of conductive plugs for respectively coupling said bias voltage to said distribution regions.

70. (Original) The system of claim 66, wherein said conductive layer comprises a conductive metallic layer.

71. (Original) The system of claim 70, wherein said conductive metallic layer has a thickness of less than or equal to 10 mil.

72. (Original) The system of claim 70, wherein said conductive metallic layer is secured to the backside of said substrate with a conductive adhesive.

73. (Canceled)

74. (Original) The system of claim 70, wherein said conductive metallic layer has a resisitivity less than 1 x 10^{-8} Ohm-meter.

75. (Original) The system of claim 70, wherein said conductive metallic layer comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

76. (Original) The system of claim 75, wherein said conductive metallic layer is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

77. (Original) The system of claim 70, wherein said conductive metallic layer has a length which exceeds a length of said substrate.

78. (Original) The system of claim 66, wherein said conductive layer comprises a cured conductive paste.

79. (Original) The system of claim 78, wherein said conductive paste has a thickness of less than or equal to 1 mil.

80. (Original) The system of claim 78, wherein said conductive paste has a resistivity less than 1 x 10^{-5} Ohm-meter.

81. (Original) The system of claim 78, wherein said conductive paste comprises a resin with conductive particles.

82. (Original) The system of claim 81, wherein said conductive paste comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

83. (Original) The system of claim 66, wherein said conductive layer comprises an isotropically conductive polymeric film.

84. (Original) The system of claim 83, wherein said conductive polymeric film has a thickness greater than 1 mil.

85. (Original) The system of claim 83, wherein said conductive polymeric film has a resistivity less than 1×10^{-5} Ohm-meter.

86. (Original) The system of claim 83, wherein said conductive polymeric film comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

87. (Original) The system of claim 66, wherein said conductive layer comprises a conductive metallic film.

88. (Original) The system of claim 87, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

89. (Original) The system of claim 87, wherein said conductive metallic film has a resistivity less than 1×10^{-5} Ohm-meter.

90. (Original) The system of claim 87, wherein said conductive metallic film comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

91. (Original) The system of claim 90, wherein said conductive metallic film is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

92. (Canceled)

93. (Original) The system of claim 92, wherein said device is a dynamic random access memory (DRAM) device.

94. (Canceled)

95. (Original) The system of claim 66, wherein said device is a processor device.

96. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate; and

an electrically conductive unbiased layer provided on a back side of said substrate, said conductive layer forming an electrical path for removing unwanted voltages and electrical noise from said substrate at a first region thereof and returning said unwanted voltages and electrical noise to said substrate at a second different region thereof to maintain a uniform bias voltage throughout the substrate.

97. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer forming an electrical path ~~between said substrate and said bias voltage source~~ thereby ~~removing~~ equalizing unwanted voltages and electrical noise ~~from~~ on said substrate between a first region of said substrate and a second different region of said substrate to maintain a uniform bias voltage throughout the substrate.

98. -100. (Canceled)

101. (Currently Amended) A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

an electrically conductive unbiased layer provided on a back side of said substrate for ~~removing~~ transferring unwanted voltages and electrical noise ~~from~~ across said substrate to maintain a uniform bias voltage throughout the substrate.

102. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

an electrically conductive unbiased layer provided on a backside of said substrate, said conductive unbiased layer forming an electrical path between a first region of said substrate and ~~said bias voltage source~~ a second region of said substrate for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

103. -104. (Canceled)